AC5S 7 level
AC6S 12.5 ms cycle

8 ms machine cycle.

1/55 cycle has also been changed.

ACS 7 level

8.00 machine cycle.

In theory, as well as practice, $3500 a chip is found.

ACS can be done with:

LEAN (CPU 160K)

LEAN (CPU 90K)

4 levels

5 levels

(1) high cost

(2) too many functions

(3) too many registers (30% used)

(4) binary part

(5) trial design

7 levels

2X the circuit

Large size

Long cable length

also contributes to cycle

(FD) machine not

Physical space

size goes ~ 4.40 chip

$\sqrt[3]{1.73} \times \text{large}

4.40 chip in ACS

$\frac{1}{5}$ of 8MS is in wires

$\frac{2}{3} = 1.6$

$\frac{1.6}{3} = 0.533$

$0.533 \times 1.732 = 0.916$

$\frac{5 + 6}{1.987} = 3.067$

$\frac{13.707}{3.067} \approx 4.490$

4.490

13.707 ms

Expected

4.40 ms

12.5 ms

13.707 ms

E: find a reasonable question for SDD

Reduce noise to fulfill 4 step: one better than software soln.

for short loop or "true" code, can fetch ahead about 2 branches

8.56

10.08

1.987

2
ACS sends more than 300
3500 ms for 180 instructions
1700 ms for 240 instructions
ACS can not be twice the cycle

PRET

Prof.

jittering

Branch

Instruction/Branch is 30, 64, 70

x is

2 as observed

data/branch

32 bit is faster (than 16-64)

30% is faster

Cost of hardware clock cycle

Scientific Job Shop

Measures of M. Brunnman:

32 bit 70% utilization 80%
64 bit 30% utilization 70%
(average 41 bit)

More in memory gives big gains in speed

25% to backing common not in ACS

5% of time in reports or in security

other issues are less

5% and 91 order was

rest follows
Can ACS really go to 6 cycles?

Sure, say they can.

If possible, new pre-computed systems.

Arbitrage, ACS is in much higher

ACS spent less money on latest case

Channel arguments were ecumenical.

Not limited to using Mod 91

Bits of I/O ~ 8 bit per instruction executed

Readability argument

Example

Kernel: 412.5 ms to do a loop

\[
\frac{288}{124.5}
\]

124.5 = 3.8% factor

\[
\frac{288}{288} = 100%
\]

would predict 56.2% faster, but on cycle time

For address bugs ~ 9%

For address with bugs ~ 5%

For repetitive bugs ~ 5%

ACS 2.5x better than ACS on busy code

1.4x better on best case
in theory, ACS seems can do no better than 90% of 360

but practice it can be much

to do better, they would have to throw out

1. preface to branch
2. 48 bit word
3. extra register
4. binary 16 point
put in AX etc.

then what is the difference??
from 360 after all these changes.

any actual mix of pure floating problem
ACCS 43% faster

if while more double in the sample

execution time ACC 43% faster (rather than 56%)
so architecture was only 9% gain

OS: (1) can run with change in OS as is
(2) improved OS? 2 categories
(a) optimizing compiler -- much in machine itself, -- hardware
compiler must do free registers allocation on ACS
(b) medium concept for OS -- can work on 360 as well.
new medium index

more of the above depends on 2 micro controllers, etc...

in the situation capability of ACC is higher than ACS, but neither here meaning

ACS 480 MIPS
ACS 500 MIPS
In principle ACS is small step backward
in practice, large " "
In terms of ASF it is enormous step backward

Sure rejects? (1) not upset problem in central code
(2) doesn't make up
(3) can be eliminated if necessary

19 525 boxes in July 91
15 are in repair

ACS: 12 lost 12 starts 48 bid sold
ACC: 8 16 32 lost
ACS rejected above 50% of

(1) ACS
(2) ACS + 360 @ 13
360 only? (This machine can be ACS or
mostly 360)

AC2 lost, not been enough
AC6 lost

not without argument

no advantage to architecture
unless there is a

What will be the measuring stick for medicine in the '70s
Summary: In practice, AEC 360 is less performant.
Cost: 1.1 x ACS

In practice, the ratio is 7:1, performant 1.4 to 3 x ACS.
Cost: 0.35 x ACS

AEC 360 can go.
ACS cannot.
It cannot fulfill.
It can be profitable.

Actual test ratios are 2:1 in favor of 360.

Market Place:

No. of customers

PV ~ \frac{1}{4} 

Limits of "band". Lower: PV price, upper: PV profit.

Cost breakthroughs.

The SP is now limited.

And memory to support max performance.

AEC 360 is a cost barrier of 85. can break.

AEC 360 is very

Queasy in space

and time.

PV is very

Queasy in space

and time.

PV is very
32 - 64 - what about 128?

5 kinds 8 mi

70% 32 ft 50% 64 ft?

80 20%

50 50?
Grundahl

On Relative Speeds in Electromagnetic Guidance:

A. 72 ft. in 60 mph speed
   - 84 mph (max. 85)
   - 75 % speed regulation
   - 75 % speed regulation in water

The regulation will be 0 to -5 % regulation on 5.