### Table 1: Single- and Double-Precision Durations

<table>
<thead>
<tr>
<th>Format</th>
<th>Single</th>
<th>Double</th>
</tr>
</thead>
<tbody>
<tr>
<td>32-bit</td>
<td>1/2</td>
<td>3/2</td>
</tr>
<tr>
<td>64-bit</td>
<td>1</td>
<td>2</td>
</tr>
</tbody>
</table>

### Comments

- The operation can lead to loss of precision.
- "Repeatable, debug"
- "Can't avoid" (possibly a typo for "can't avoid")
- "Can only be single precision" for 32-bit operations.
- "Corrupt in 32-bit but not in 64-bit. This shows the ACS can be 48-bit but not 32-bit in a single precision environment".

### Timing: DTP Code

- **ACS**: 32 cycles with 400 ns.
- **NSC**: 296 ns.

### Summary

- Assume 8 floating point regs.
- Assumed to fit in memory.
- 0 use: operands $AD(J,K)$, $AA(I)$, $AB(I)$.
(2) branching: testing in advance?

- many ways can be used to do this on branching
- ACS microcode is 7 cycles to prepare to branch.
- 14-21 cycles

- for many branches, little gain
- for branches, little gain

- one can look for branches
- a little saving
- to greatest of game

- e.g. DIF, S branches in loop
  - 14 cycles more spent on instruction
  - (only if could have been removed)

(3) carefully use & combine to avoid load stage usage...
- sequence statements
- interleave usage, etc.
- Seems can be done
- controllably
- optimization is easier than ACS, e.g. branches aren't
  moved ahead.

(4) % of registers:
- RX instruction uses reg for it's reg & about 1/2, 8 rega
  ACS can see from rega - available to use & refilled from
  no enough

- only 1/2 more reg to reg in practice
- not enough
(6) and not have to trap a lot II
probably built in shelf

(7) composition can't use. This -- either good for our customers

(5) flexigrip part: 

anomalies are being fixed now

(7) O is above -- investment can be
put into improving ACS and it is there + getting off

851" complete

peakulpile: 500 kg

(7) Flexigrip Composition

[2.7 x random dimensions chisel with 13.5 rag]

(6) Field of Compet.

(11) Multiple dust collectors?
they plan to offer 17 dust collectors. escort high-speed req.

(10) what looked at ACS, it now available, in half

(6) 5/360 width checked at ACS, it now available,
not done. unfortunately the keystone is not in the case -- it will included, indeed, something useful
conservative code copying -- only use if genuine need.
for bad code substitutions -- branch even
a 2nd instruction will raise rate.

156: smaller HS show shorter access times
early load of branches ... IC9, late time with this IC8
1.4 X faster on bad code causes

average: \( \frac{1}{\text{rate}} \)  
constant