FHP vs Intel 432
Competitive Analysis
FHP ARCHITECTURAL ADVANTAGES OVER iAPX 432

Data services

- Much larger object size limit (FHP: 256Mb, iAPX 432: 64Kb).
- Memory management policies totally hidden.
- Ability to access files as objects.
- Totally separate addressing and protection models.
- Object identifiers wide enough to be true UIDs.
- Object identifiers not scarce, so no need to reclaim them.
- Bit-granular addressing supported directly.

Instruction services

- Very regular and predictable I-stream.
- Operand addressing has NO side effects.
- Single-instruction compare/branch and loop control.
- Direct support of string data through Name Table.
- Direct support of non-homogeneous arrays (tables).
- Full decimal repertoire (all types and lengths).
- Multiple S-languages.

Process services

- Extraordinarily fast Neighborhood Call.
- Accelerated argument transmission.
- Not limited to one static data segment per process.
FHP ENVIRONMENTAL ADVANTAGES OVER iAPX 432

Maturity

- Architecture has had two major iterations.
- SPL is an effective systems programming language with a mature compiler that produces excellent code.
- Effective SPL coding practices have been defined.
- Performance metrics and tools are defined and available.

Traditional programming support

- Objects function well as large address spaces.
- IBM-format floating point preserves DG compatibility.
- Language breadth: FORTRAN, COBOL, PL/I
- State-of-the-art compilers and binders

Performance support

- Possibility of user microprogramming
- Wide range of binding options for performance

System issues

- Paged VM and object growth implemented
- OS scheduling and synchronization tools less rigid
ADVANTAGES COMMON TO FHP AND IAPX 432

Data services

- Segmented address space, as opposed to flat address spaces (M68000, VAX, MV/8000).

- Totally shared address space. Neither machine is confined to a per-process or per-processor address space.

- Robust (though very different) protection schemes. FHP uses Access Control Lists, iAPX 432 capabilities.

Instruction services

- Three-address, memory-to-memory architecture.

- Wide variety of signed and unsigned integer data types.

- Operators and operand addressing totally orthogonal.

Environmental issues

- System primitives accelerated into microcode.

- Very high-level systems language. iAPX 432 will use Ada. FHP uses SPL (similar to Ada).
### COMPETITIVE POSITIONING

<table>
<thead>
<tr>
<th>Competition</th>
<th>Complexity (No. of devices)</th>
<th>Chip Set Performance</th>
<th>Product Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fujitsu (16-bit μproc)</td>
<td>40,000</td>
<td>16-bit multiply, 32-bit result in 9.75 μsec</td>
<td>Production in 1980</td>
</tr>
<tr>
<td>Motorola (16-bit μproc)</td>
<td>70,000</td>
<td></td>
<td>Production in 1980</td>
</tr>
<tr>
<td>VLSI FHP (32-bit μproc)</td>
<td>100,000</td>
<td>32-bit multiply in 2.25 μsec; accumulator to memory add in 0.5 μsec</td>
<td>1985?</td>
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<tr>
<td>HP (32-bit μproc)</td>
<td>450,000</td>
<td>32-bit multiply in 1.8 μsec</td>
<td>Experimental</td>
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<tr>
<td>Bell Labs (32-bit μproc)</td>
<td>100,000</td>
<td>reg. to reg. add in .375 μsec</td>
<td>Soon</td>
</tr>
<tr>
<td>Intel 432 (32-bit μproc)</td>
<td>50,000-100,000</td>
<td>32-bit multiply in 6.25 μsec</td>
<td>Samples</td>
</tr>
</tbody>
</table>

### ANALYSIS

- VLSI FHP is competitive with both the Bell Labs and HP experimental products.

- Primary visible competition is the Intel 432. Based on device level performance, VLSI FHP is more than competitive with the current 432.

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