Architecture at HP:
Two Decades of Innovation

Joel S. Birnbaum

Microprocessor Forum
San Jose, CA
October 14, 1997

Computer Architecture at HP

- A summary of motivations, innovations and implementations in the period 1981 to the present
- Some observations about emerging systems requirements for the next decade and ongoing research to address them

A Capsule History

The 80s:

- RISC consolidation and evolution
- Spectrum, HP Precision Architecture, and PA-RISC
- Migration from HP 3000, 1000, M68000 architectures

The Early 90s:

- Beyond RISC: The quest for concurrency
- Superscalar, VLIW, Wide Word
- Compatibility with PA-RISC

1994 - Present:

- The Intel alliance
- Next generation technology and IA-64

WHAT'S NEXT?...

Precision Architecture Principles

- Compiler does what it does best
- Hardware does what it does best
- As simple as possible, but not simpler
- Measure / justify everything
  - Optimize for application throughput
  - Most work in least time
- Architecture scales across family of implementations
- Seamless migration essential

Technology Enablers of RISC Architecture

- Progress in VLSI: Fast registers, cache
- Globally optimizing compilers
- Performance measurement and analysis tools

Challenges of RISC Architecture

- Compiler accuracy and reliability
- Migration of legacy code

Major PA-RISC Innovations

- Compound instructions based on usage statistics
- Instruction nullification
- Legacy software migration
  - Binary code translation
  - Millicode
  - Migration centers
- 64-bit addresses
  - 32-bit segments
- Graphics and multimedia extensions

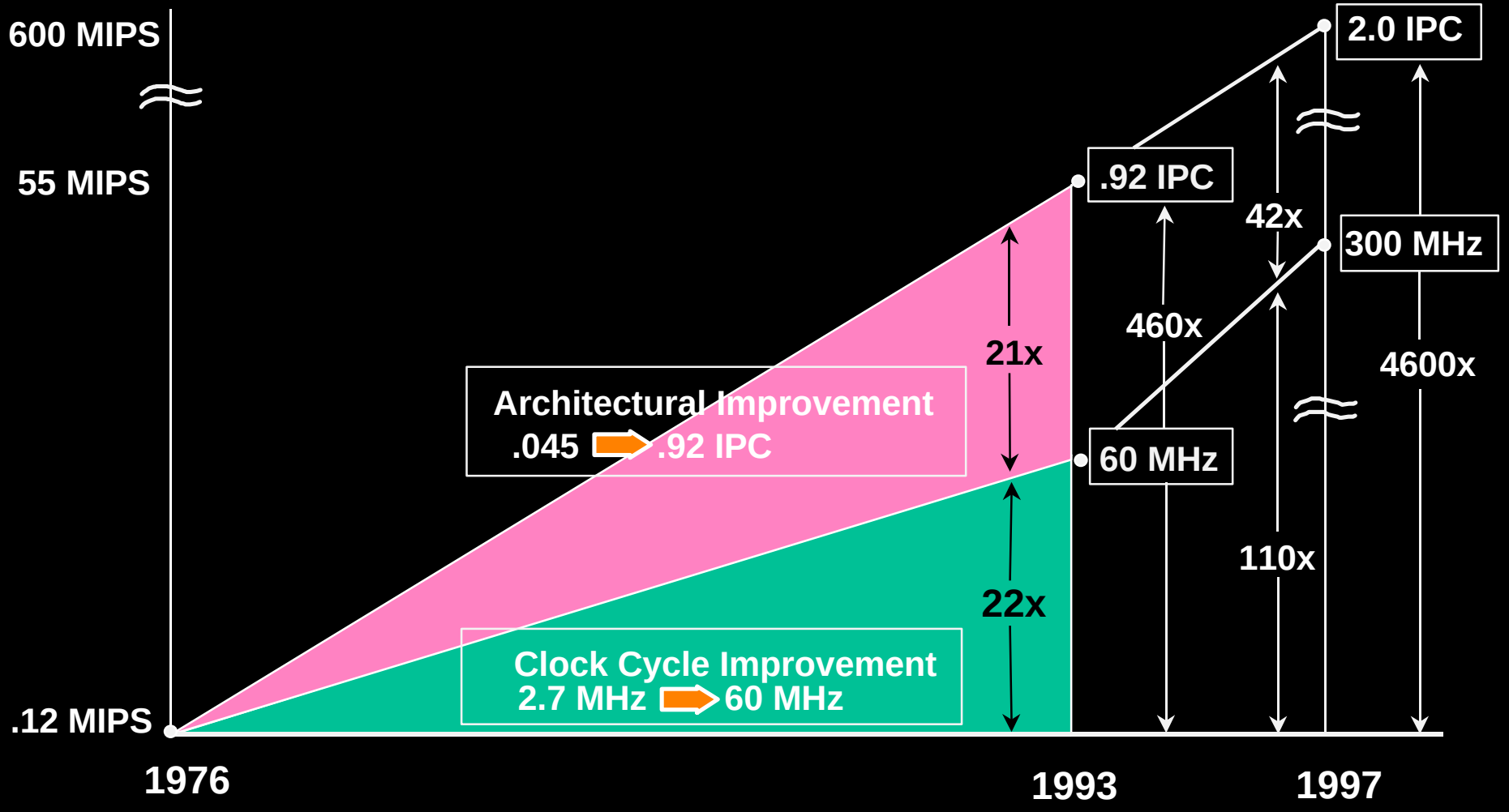
Why a New Architecture?

- Insatiable demand for more performance
- Processor/memory speed gap implications
  - Higher bandwidth
  - More registers
  - Overlapped memory latencies
- Need for greater number of instructions per cycle
- Diminishing gains from growing microprocessor design complexity

Industry Solutions

- Superscalar RISC
  - Improved ILP, but:
    - Significant hardware complexity
    - Not transparent to compiler
    - Asymptotic IPC of 1.5 - 3
- VLIW, Vector Architectures
  - Even higher ILP
    - Explicit parallelism
    - Parallelizing compilers
  - But limited applicability, scalability, and compatibility
- Drives the need for a new architecture

Microprocessor Performance Growth

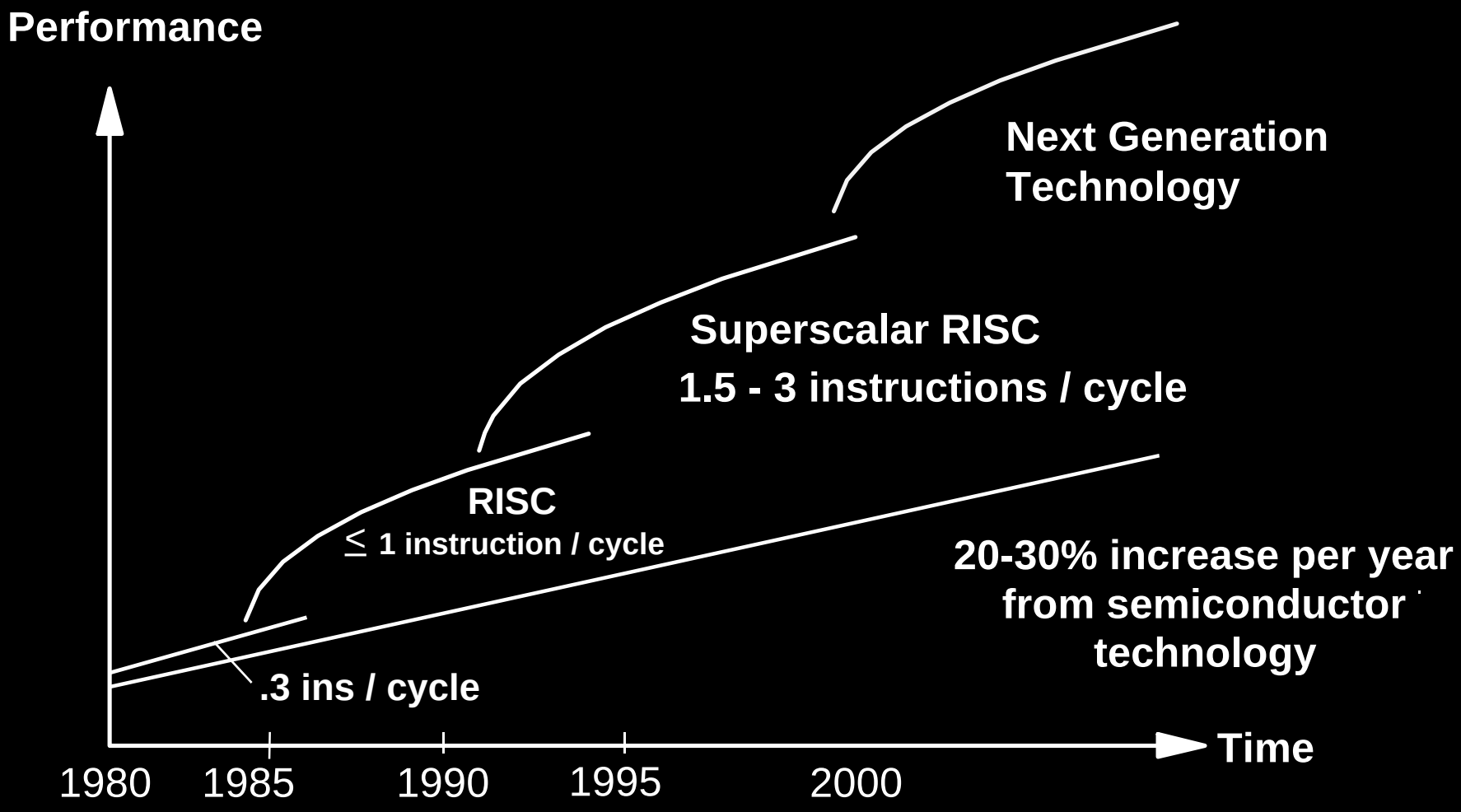


Source: IEEE Spectrum (1989) (1976-1993)

Major Conclusion: High ILP Needs a New Architectural Approach

- High ILP requires explicitly scheduled code
  - Scheduling by compiler
- Architecture must expose parallelism
- Scalability across implementations and applications required

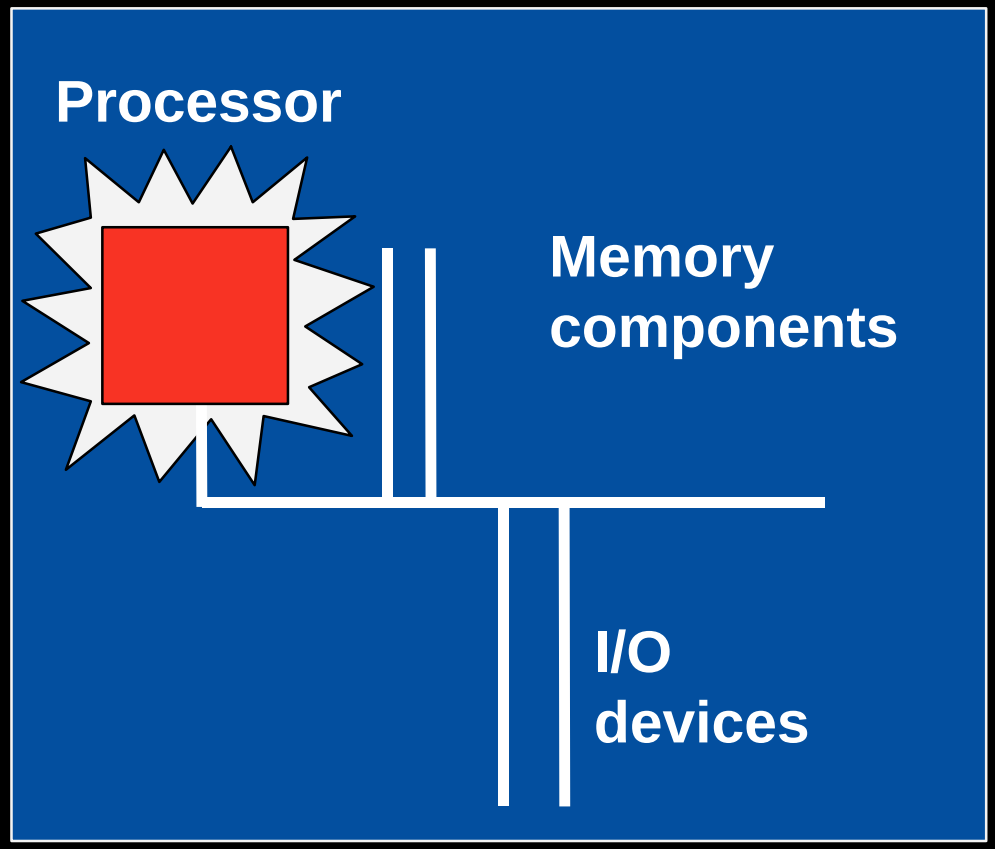
IPC Evolution from Architecture and Microarchitecure



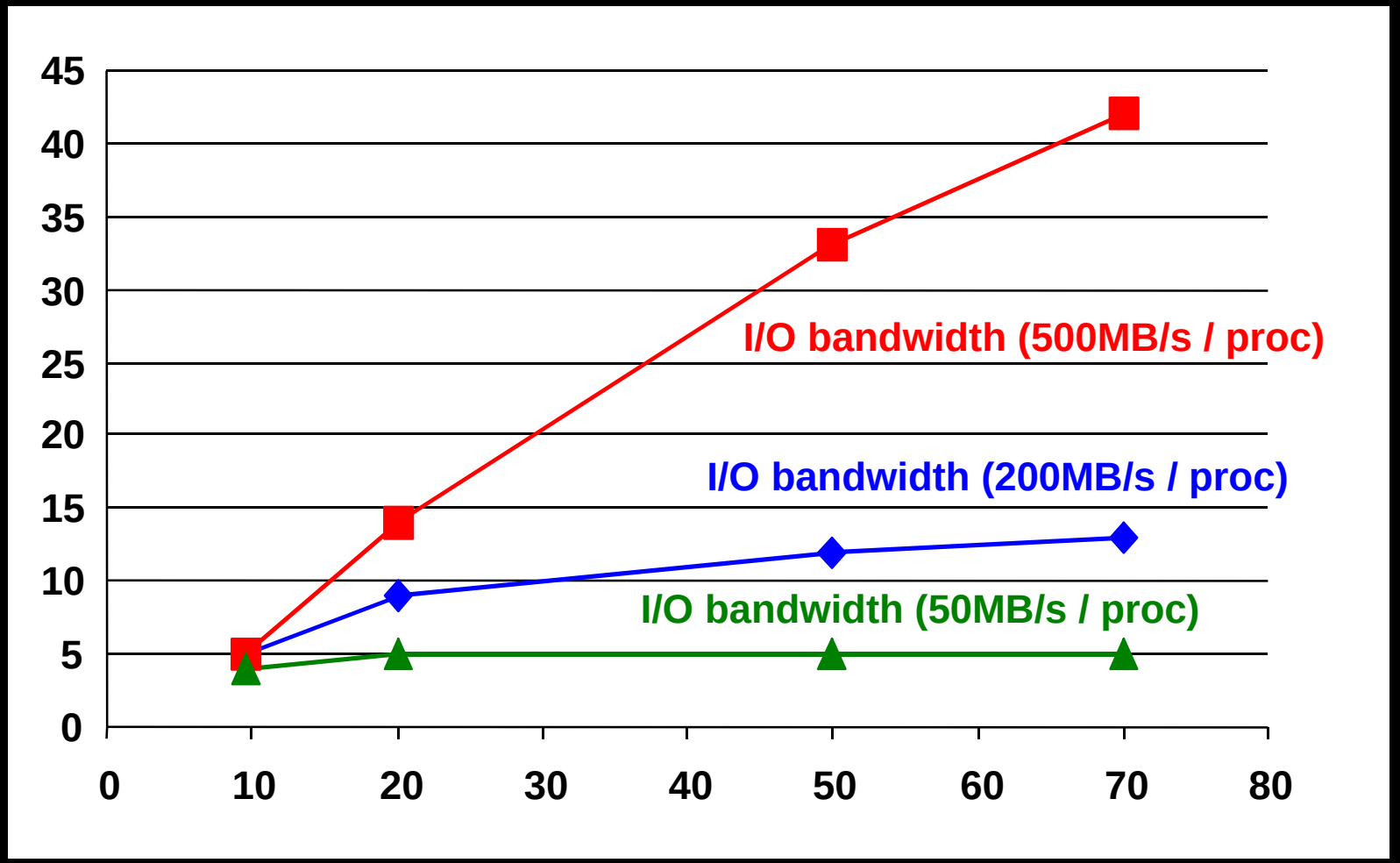
Need for a New Industry-Standard Architecture

- HP alone would not succeed with a new proprietary architecture: economics, acceptance by ISVs
- Technology alliance melds architecture/ design / fabrication excellence of Intel with architecture and systems excellence of HP
- Opportunity for scalable common hardware platforms across operating systems

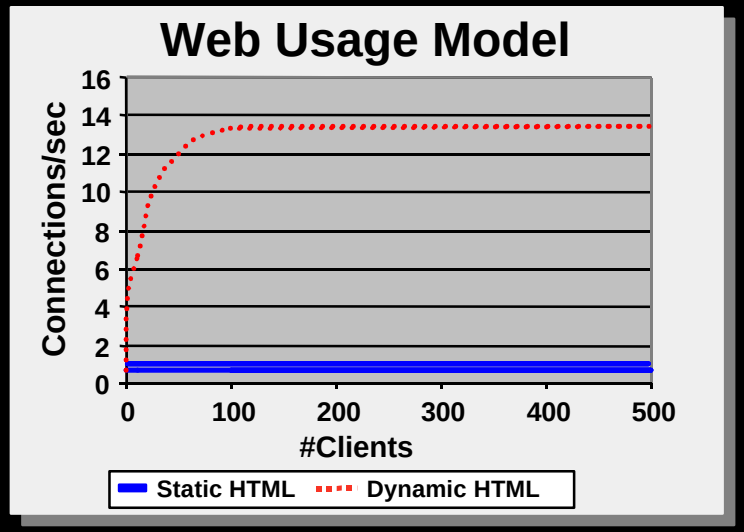
The Rest of the System?

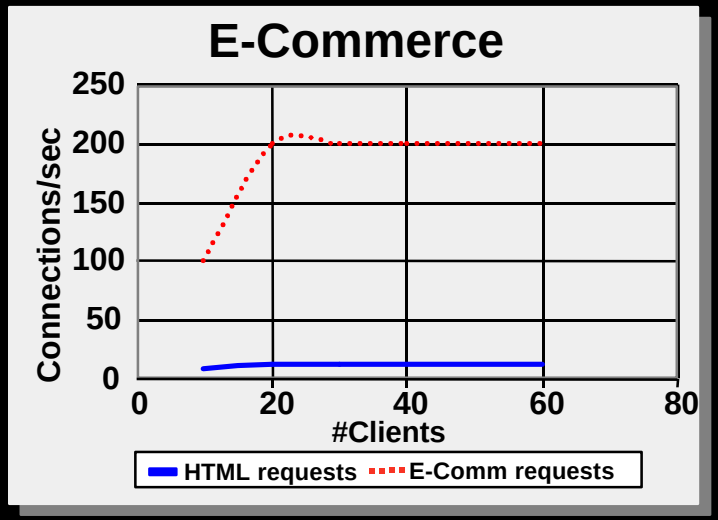


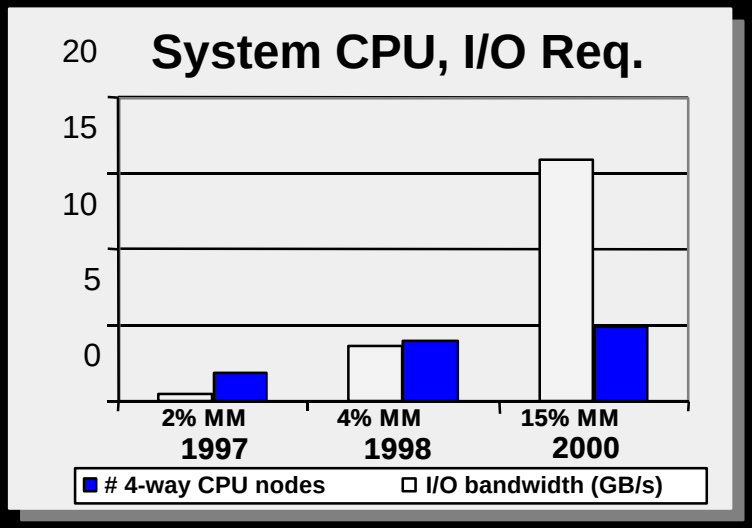
The Rest of the System



Changing Workloads

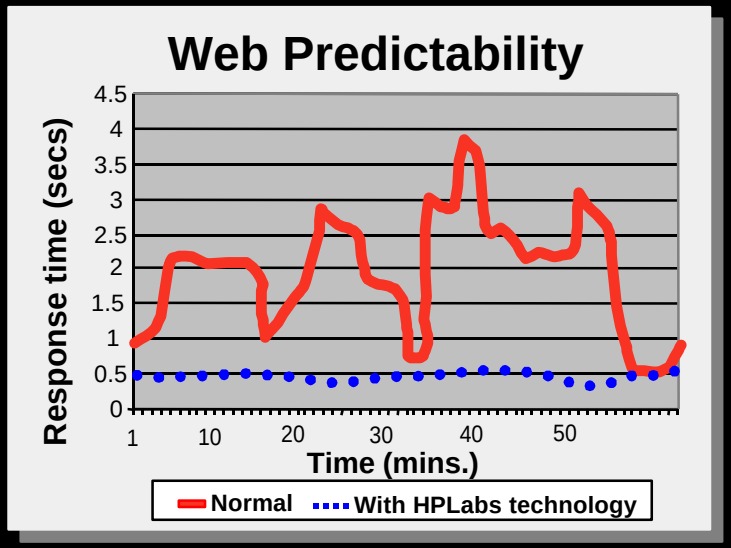


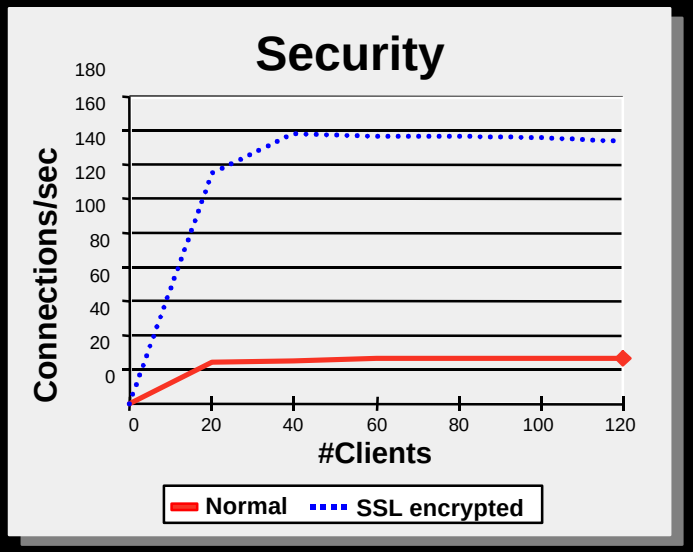


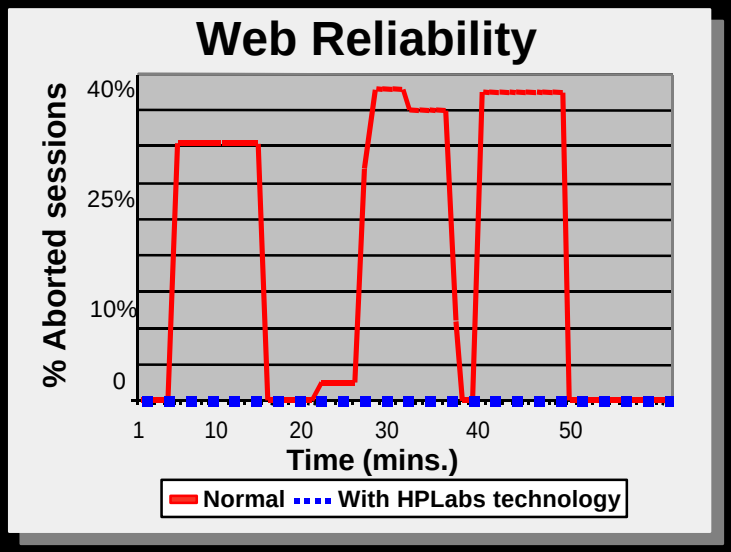


- ***Increasing system loads***
- ***Increasing system bandwidth requirements***

New Cost-Value Measures

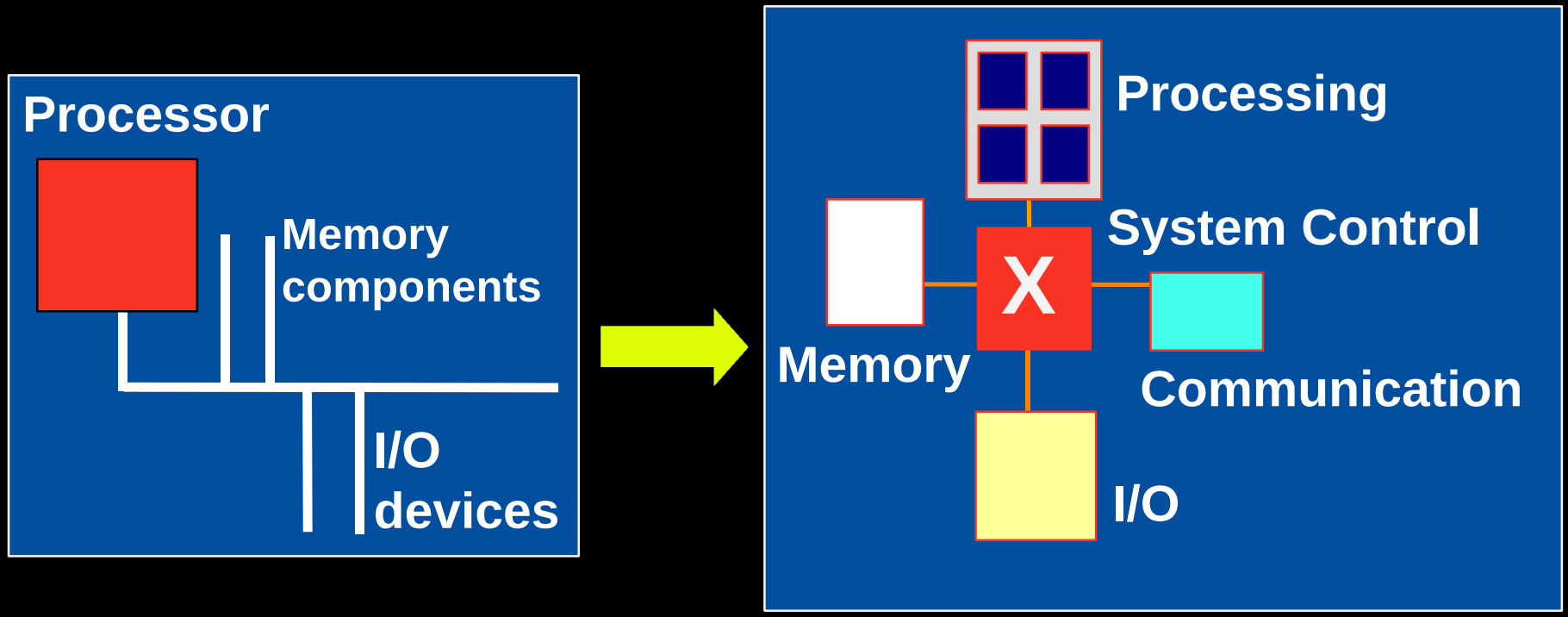






- ***Need mechanisms for predictability, security, reliability***

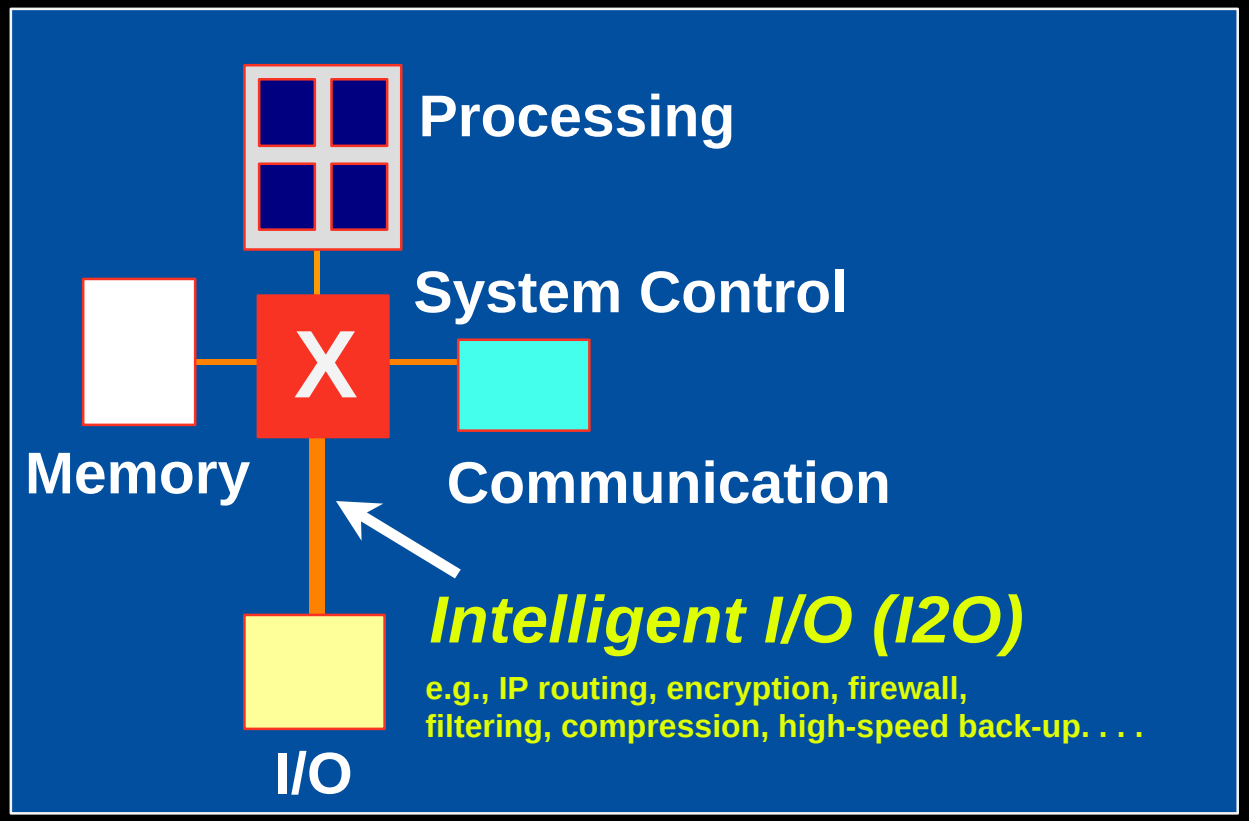
New Control Points



Processor-centric → Semi-autonomous Subsystems

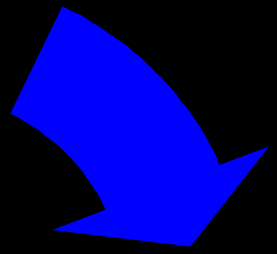
New Control Points

… in an open industry standard framework that permits system value adds



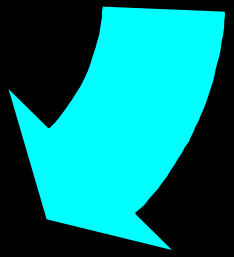
The New Challenges

Computing Components



- Semi-autonomous subsystems
- Integrated communication, memory, and computation

Computing Systems



- Distributed, heterogeneous systems of systems

Computing Services

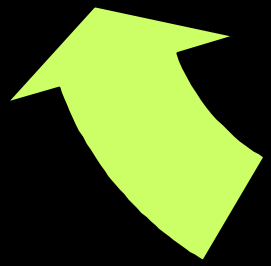
(Information and Computation "Utilities")

The New Challenges

Computing Components

- Custom (embedded) processors
- New control points

Computing Systems



- Information appliances
- Utility servers

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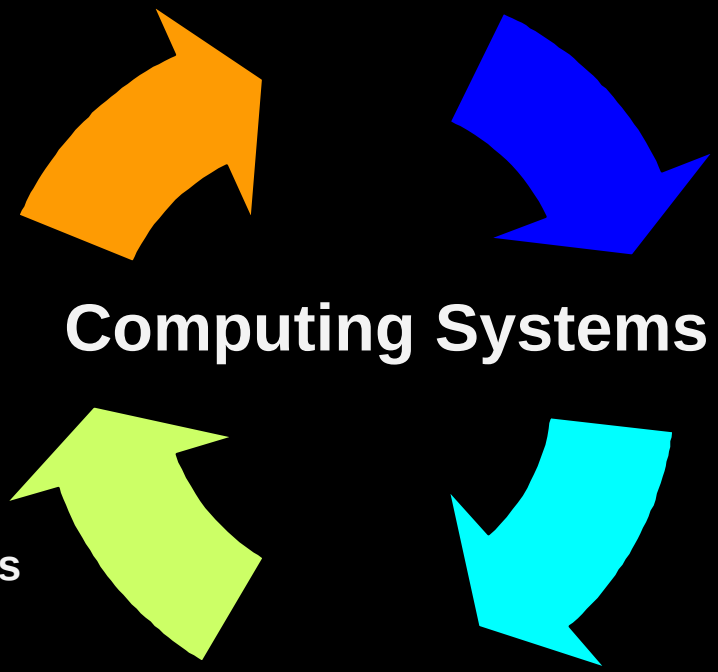

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HP Labs is focused on the new challenges of tomorrow