Cell Design and Layout

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Adapted from EE271 notes,
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Overview

- Wires
- FPGA
- Gate Array
- Standard Cell
- Datapath Cells
- Cell Layout
- Reading
  - W&E 6.3-6.3.6, 5.3
Wires

- Part of capacitive load
  - Need to know the length to size (driver) gates
  - Need to plan for it

- Resistance
  - Long wires have RC time constants

- Special wires
  - Power, ground, and clock
  - Need to have low resistance
## Wire Properties

<table>
<thead>
<tr>
<th>Layer</th>
<th>Resistance</th>
<th>Capacitance</th>
<th>Connects to</th>
</tr>
</thead>
<tbody>
<tr>
<td>M2</td>
<td>Low</td>
<td>Low</td>
<td>M1</td>
</tr>
<tr>
<td>M1</td>
<td>Low</td>
<td>Low</td>
<td>diff,poly,M2</td>
</tr>
<tr>
<td>poly</td>
<td>Medium</td>
<td>Low</td>
<td>gate,M1</td>
</tr>
<tr>
<td>ndiff</td>
<td>Medium</td>
<td>High</td>
<td>S/D,M1</td>
</tr>
<tr>
<td>pdiff</td>
<td>Medium</td>
<td>High</td>
<td>S/D,M1</td>
</tr>
</tbody>
</table>
Wire Characteristics

\[ R = \frac{\rho}{t} \frac{L}{W} = R^{sq} \frac{L}{W} \]

<table>
<thead>
<tr>
<th>Layer</th>
<th>R.</th>
<th>( R. /R_{\text{trans}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>metal</td>
<td>0.1Ω</td>
<td>1/1.5x10^5</td>
</tr>
<tr>
<td>poly</td>
<td>5Ω</td>
<td>1/3000</td>
</tr>
<tr>
<td>ndiff</td>
<td>5Ω</td>
<td>1/3000</td>
</tr>
<tr>
<td>pdiff</td>
<td>5Ω</td>
<td>1/3000</td>
</tr>
<tr>
<td>nMOS</td>
<td>15KΩ</td>
<td>1</td>
</tr>
<tr>
<td>pMOS</td>
<td>30KΩ</td>
<td>2</td>
</tr>
</tbody>
</table>
Wire Usage

- **Diffusion**
  - Bad wire (high capacitance)
  - Only used to connect to transistors

- **Poly**
  - Resistance high: good for short, local interconnects
  - Do not use to route outside cells or as jumpers in long wires

- **Metal**
  - M1: only conductor that can connect to poly and diff
  - M1,...,M_{n-1} for general wiring
  - M_n for V_{dd}, Ground, and clock routing
Cell Implementation Technologies

- **Field programmable gate arrays (FPGA)**
  - Chips prefabricated; program fuses/anti-fuses

- **Gate arrays (mask programmable)**
  - Transistors prefabricated; customize metal to generate cells

- **Standard cells**
  - All cells have fixed height
  - Wiring may be restricted to channels

- **Macro cells**
  - Similar to standard cells but
  - Wiring done over cells

- **Memory (2D array)**
FPGA

- Logic is programmed into chip after fabrication
- Programming done using
  - Memory cells and CMOS switches
  - Fuse/anti-fuse
  - EPROM cells hold values for 10 years
- Customizing wires
  - To program connections, need switches
  - Switches have R and C; slows down signals on wires
- Completely prefabricated in large volume
  - Cost effective for certain applications
FPGA Wiring

- Standard cell like wiring (with channels)
  - Each channel has wires of different length
  - How many of each length determined by design statistics
  - Use logic blocks as repeaters when necessary
  - **Problem:** switches in wires (high resistance)
Gate Array

- Transistors predefined
  - W/L all the same (or choice limited)
  - Transistors prefabricated
  - Chip covered with transistors (sea of gates)
- Designer provides metal patterns that form logic gates by connecting transistors
  - Transistors under wiring channels not used. Why?
- Cheaper and faster to manufacture than standard cells. Why?
Gate Array Layout

2-input NAND

V_{dd} A B V_{dd}

Gnd out Gnd

2-input NAND
Standard Cell

- Appropriate for all or part of a custom chip
- All cells have the same height (with abutting power and ground)
- Cells tiled into rows
- Rows separated by routing channels
  - Channel height variable

Cell Height
(includes $V_{dd}$, Gnd)

Channel height
Standard Cell Layout Example
Macro Cell

- Standard cell with wiring done inside cell
  - 1D - datapath
  - 2D - memory
- Wires kept short and regular
  - Less wiring area
  - Less wire load (drivers can be smaller)
  - Order cells to minimize wire lengths
Datapath

- Fixed height cells with bit pitch set to
  - height of tallest cell
  - accommodate the total number of over-the-cell wires per bit
  - $128\lambda$ a good choice
- Often, cells are **mirrored** (every other cell is flipped vertically) to share $V_{dd}$ and Gnd rails. Why?
- Some cells take up multiple bit pitches
  - E.g., 4-bit Manchester carry chain

- Variable width
  - Depends on functionality of cells
Datapath (continued)

- Wires over cells
  - Bit lines for data
  - Word lines for control, clock

- Place cells to minimize number of horizontal tracks and wire lengths

![Slice Plan](image)

Requires 3 Tracks
Basic Layout Guidelines

- Do wire planning before cell layout
  - Assign preferred direction to each layer
  - Group p’s and n’s
  - Determine input/output port locations
  - Power, ground, and clock wires must be wide

- Determine cell pitch
  - Height of tallest cell
  - Number of over-the-cell tracks and wire lengths

- Use metal for wiring
  - Use poly for intra-cell wiring only
  - Use diffusion for connection to transistors only

- Do stick diagram first!
Basic Cell Layout Guidelines

- P-N spacing is large, so keep pMOS together and nMOS together
  - Mirror cells, if necessary. How does it help?

- $V_{dd}$ and ground distribution must be in wide metal
  - $V_{dd}$ runs near pMOS groups
  - Ground runs near nMOS groups

- Layers in alternate directions
  - M1 and M2 should run in (predominantly) orthogonal directions. Why?
Transistor Layout

- Transistors should be at least as wide as contacts \((4\lambda)\)
- Use as many contacts as possible for wider transistors
- Don’t use \(3\lambda\) device except for weak devices
Transistor Folding

- Better aspect ratio for large transistors
- Reduces diffusion area
Folding Series Gates

- Fold the whole stack, not individual transistors
Example: Standard Cell Latch

- Static design
- $\Phi'$ generated internally
- Feedback isolated from output

\[ \Phi \quad in \quad out \]
Standard Cell Stick Diagram

- Local poly routing
- Transistors share diffusion
- Room for M2 track over cell

Symbols:
- clk
- in
- out
- V_{dd}
- Gnd
Standard Cell Layout
Datapath Cell Layout Options

- Data/control
  - Data bus in M1 and control in M2
  - Data bus in M2 and control in M1

- Power/Ground
  - in control direction (vertical)
  - in data direction (horizontal)
Stick Diagram (1)

- Start with just wires

\[ \text{V}_{dd} \quad \text{ST} \quad \text{ST}' \quad \text{RD} \quad \text{RD}' \]

\[ \text{Gnd} \quad \text{D}_{IN} \quad \text{D}_{OUT} \]
Stick Diagram (2)

- Draw transistors connected to inputs and outputs
Stick Diagram (3)

- Draw remaining transistors
Power and Ground

- Resistance of power supply line must be very small
  - If too large, then the voltage supplied to gates will drop (*why*?), which may cause malfunction of gates
  - So, power supply lines must be *wide* metal
    - \( R_{\text{trans}} \gg R_{\text{metal}} \)
    - Not so easy since wires are long and transistors are large
Power IR Drop

- Example: for 100K gate chip
  - Each gate drives 1mm wire (200fF) in 500ps
    - $I = C \frac{dV}{dt} = 200fF \times \frac{2.5V}{500ps} = 1mA$
    - If all switch at once, 100A!
    - Even if only 10% switch at once, still 10A peak current!
- Considerable IR drop!
  - Need many supply pins, wide power supply wires
  - Grids are good for low $R$
Power Distribution

- Distribute power on thickest metal

local buses